**ANALOG DEVICES**

# Low Cost, Low Power Video Op Amp

# AD818

## FEATURES
**Low Cost**
**Excellent Video Performance**
- **55 MHz 0.1 dB Bandwidth (Gain = +2)**
- **0.01% & 0.05° Differential Gain & Phase Errors**

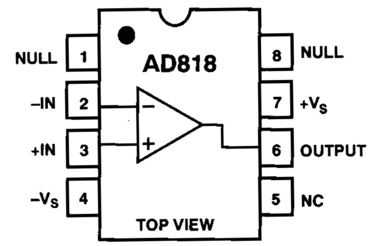
**High Speed**
- **130 MHz Bandwidth (3 dB, G = +2)**
- **100 MHz Bandwidth (3 dB, G+ = −1)**
- **500 V/µs Slew Rate**
- **80 ns Settling Time to 0.01% ($V_O$ = 10 V Step)**

**High Output Drive Capability**
- **50 mA Minimum Output Current**
- **Ideal for Driving Back Terminated Cables**

**Flexible Power Supply**
- **Specified for Single (+5 V) and Dual (±5 V to ±15 V) Power Supplies**
- **Low Power: 7.5 mA max Supply Current**

**Available in 8-Pin SOIC and 8-Pin Plastic Mini-DIP**

## CONNECTION DIAGRAMS
**8-Pin Plastic Mini-DIP (N), and SOIC (R) Packages**




NC = NO CONNECT

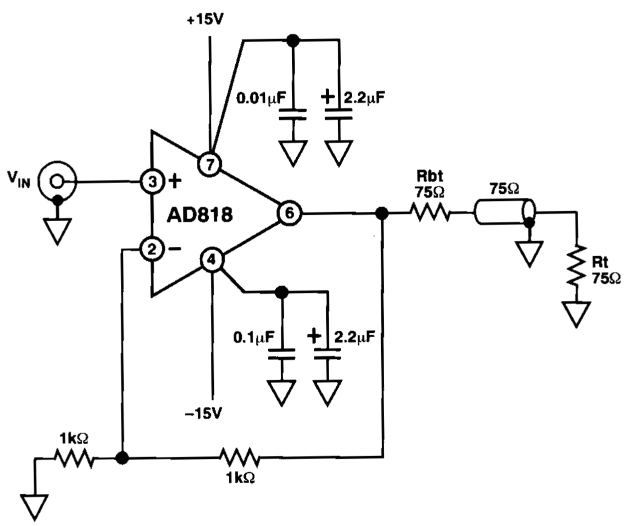
## PRODUCT DESCRIPTION
The AD818 is a low cost, video op amp optimized for use in video applications which require gains equal to or greater than +2 or −1. The AD818 low differential gain and phase errors, single supply functionality, low power and high output drive make it ideal for cable driving applications such as video cameras and professional video equipment.

With video specs like 0.1 dB flatness to 55 MHz and low differential gain and phase errors of 0.01% and 0.05°, along with 50 mA of output current, the AD818 is an excellent choice for any video application. The 130 MHz 3 dB bandwidth (G = +2) and 500 V/µs slew rate make the AD818 useful in many high speed applications including: video monitors, CATV, color copiers, image scanners and fax machines.

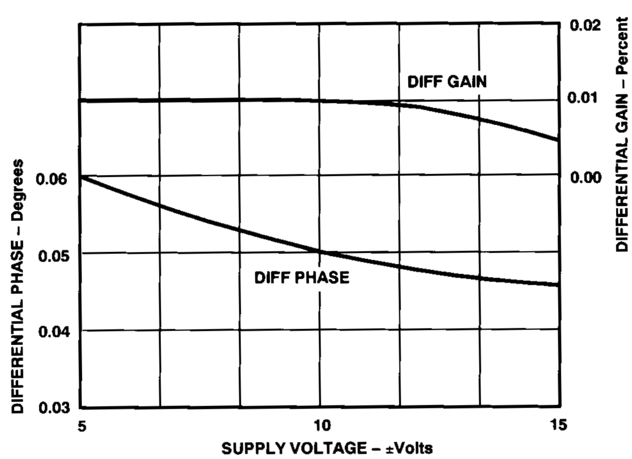
The AD818 is fully specified for operation with a single +5 V power supply and with dual supplies from ±5 V to ±15 V. This power supply flexibility, coupled with a very low supply current of 7.5 mA and excellent ac characteristics under all power supply conditions, make the AD818 the ideal choice for many demanding yet power sensitive applications.

The AD818 is a voltage feedback op amp and excels as a gain stage in high speed and video systems (gain = >2 or −1). It achieves a settling time of 45 ns to 0.1%, with a low input offset voltage of 2 mV max.

The AD818 is available in low cost, small 8-pin plastic mini-DIP and SOIC packages.




*AD818 Video Line Driver*




*AD818 Differential Gain and Phase vs. Supply*

REV. A




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# AD818—SPECIFICATIONS (@ $T_A$ = +25°C, unless otherwise noted)

| Parameter | Conditions | $V_S$ | AD818A Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | | |
| −3 dB Bandwidth | Gain = +2 | ±5 V | 70 | 95 | | MHz |
| | | ±15 V | 100 | 130 | | MHz |
| | | 0, +5 V | 40 | 55 | | MHz |
| | Gain = −1 | ±5 V | 50 | 70 | | MHz |
| | | ±15 V | 70 | 100 | | MHz |
| | | 0, +5 V | 30 | 50 | | MHz |
| Bandwidth for 0.1 dB Flatness | Gain = +2 | ±5 V | 20 | 43 | | MHz |
| | $C_C$ = 2 pF | ±15 V | 40 | 55 | | MHz |
| | | 0, +5 V | 10 | 18 | | MHz |
| | Gain = −1 | ±5 V | 18 | 34 | | MHz |
| | $C_C$ = 2 pF | ±15 V | 40 | 72 | | MHz |
| | | 0, +5 V | 10 | 19 | | MHz |
| Full Power Bandwidth[1] | $V_{OUT}$ = 5 V p-p, $R_{LOAD}$ = 500 Ω | ±5 V | | 25.5 | | MHz |
| | $V_{OUT}$ = 20 V p-p, $R_{LOAD}$ = 1 kΩ | ±15 V | | 8.0 | | MHz |
| Slew Rate | $R_{LOAD}$ = 1 kΩ | ±5 V | 350 | 400 | | V/µs |
| | Gain = −1 | ±15 V | 450 | 500 | | V/µs |
| | | 0, +5 V | 250 | 300 | | V/µs |
| Settling Time to 0.1% | −2.5 V to +2.5 V | ±5 V | | 45 | | ns |
| | 0 V–10 V Step, $A_V$ = −1 | ±15 V | | 45 | | ns |
| to 0.01% | −2.5 V to +2.5 V | ±5 V | | 80 | | ns |
| | 0 V–10 V Step, $A_V$ = −1 | ±15 V | | 80 | | ns |
| Total Harmonic Distortion | $F_C$ = 1 MHz | ±15 V | | 63 | | dB |
| Differential Gain Error | NTSC | ±15 V | | 0.005 | 0.01 | % |
| (Rl = 150 Ω) | Gain = +2 | ±5 V | | 0.01 | 0.02 | % |
| | | 0, +5 V | | 0.08 | | % |
| Differential Phase Error | NTSC | ±15 V | | 0.045 | 0.09 | Degrees |
| (Rl = 150 Ω) | Gain = +2 | ±5 V | | 0.06 | 0.09 | Degrees |
| | | 0, +5 V | | 0.1 | | Degrees |
| Cap Load Drive | | | | 10 | | pF |
| INPUT OFFSET VOLTAGE | | ±5 V to ±15 V | | 0.5 | 2 | mV |
| | $T_{MIN}$ to $T_{MAX}$ | | | | 3 | mV |
| Offset Drift | | | | 10 | | µV/°C |
| INPUT BIAS CURRENT | | ±5 V, ±15 V | | 3.3 | 6.6 | µA |
| | $T_{MIN}$ | | | | 10 | µA |
| | $T_{MAX}$ | | | | 4.4 | µA |
| INPUT OFFSET CURRENT | | ±5 V, ±15 V | | 25 | 200 | nA |
| | $T_{MIN}$ to $T_{MAX}$ | | | | 500 | nA |
| Offset Current Drift | | | | 0.3 | | nA/°C |
| OPEN-LOOP GAIN | $V_{OUT}$ = ±2.5 V | ±5 V | | | | |
| | $R_{LOAD}$ = 500 Ω | | 3 | 5 | | V/mV |
| | $T_{MIN}$ to $T_{MAX}$ | | 2 | | | V/mV |
| | $R_{LOAD}$ = 150 Ω | | 2 | 4 | | V/mV |
| | $V_{OUT}$ = ±10 V | ±15 V | | | | |
| | $R_{LOAD}$ = 1 kΩ | | 6 | 9 | | V/mV |
| | $T_{MIN}$ to $T_{MAX}$ | | 3 | | | V/mV |
| | $V_{OUT}$ = ±7.5 V | ±15 V | | | | |
| | $R_{LOAD}$ = 150 Ω (50 mA Output) | | 3 | 5 | | V/mV |
| COMMON-MODE REJECTION | $V_{CM}$ = ±2.5 V | ±5 V | 82 | 100 | | dB |
| | $V_{CM}$ = ±12 V | ±15 V | 86 | 120 | | dB |
| | $T_{MIN}$ to $T_{MAX}$ | ±15 V | 84 | 100 | | dB |
| POWER SUPPLY REJECTION | $V_S$ = ±5 V to ±15 V | | 80 | 90 | | dB |
| | $T_{MIN}$ to $T_{MAX}$ | | 80 | | | dB |
| INPUT VOLTAGE NOISE | f = 10 kHz | ±5 V, ±15 V | | 10 | | nV/√Hz |
| INPUT CURRENT NOISE | f = 10 kHz | ±5 V, ±15 V | | 1.5 | | pA/√Hz |

| Parameter | Conditions | $V_S$ | AD818A Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| INPUT COMMON-MODE VOLTAGE RANGE | | ±5 V | +3.8 | +4.3 | | V |
| | | | −2.7 | −3.4 | | V |
| | | ±15 V | +13 | +14.3 | | V |
| | | | −12 | −13.4 | | V |
| | | 0, +5 V | +3.8 | +4.3 | | V |
| | | | +1.2 | +0.9 | | V |
| OUTPUT VOLTAGE SWING | $R_{LOAD}$ = 500 Ω | ±5 V | 3.3 | 3.8 | | ±V |
| | $R_{LOAD}$ = 150 Ω | ±5 V | 3.2 | 3.6 | | ±V |
| | $R_{LOAD}$ = 1 kΩ | ±15 V | 13.3 | 13.7 | | ±V |
| | $R_{LOAD}$ = 500 Ω | ±15 V | 12.8 | 13.4 | | ±V |
| | $R_{LOAD}$ = 500 Ω | 0, +5 V | +1.5, +3.5 | | | V |
| Output Current | | ±15 V | 50 | | | mA |
| | | ±5 V | 50 | | | mA |
| | | 0, +5 V | 30 | | | mA |
| Short-Circuit Current | | ±15 V | | 90 | | mA |
| INPUT RESISTANCE | | | | 300 | | kΩ |
| INPUT CAPACITANCE | | | | 1.5 | | pF |
| OUTPUT RESISTANCE | Open Loop | | | 8 | | Ω |
| POWER SUPPLY | | | | | | |
| Operating Range | Dual Supply | | ±2.5 | | ±18 | V |
| | Single Supply | | +5 | | +36 | V |
| Quiescent Current | | ±5 V | | 7.0 | 7.5 | mA |
| | $T_{MIN}$ to $T_{MAX}$ | ±5 V | | | 7.5 | mA |
| | | ±15 V | | | 7.5 | mA |
| | $T_{MIN}$ to $T_{MAX}$ | ±15 V | | 7.0 | 7.5 | mA |

NOTE
[1]Full power bandwidth = slew rate/2 π $V_{PEAK}$.
Specifications subject to change without notice.

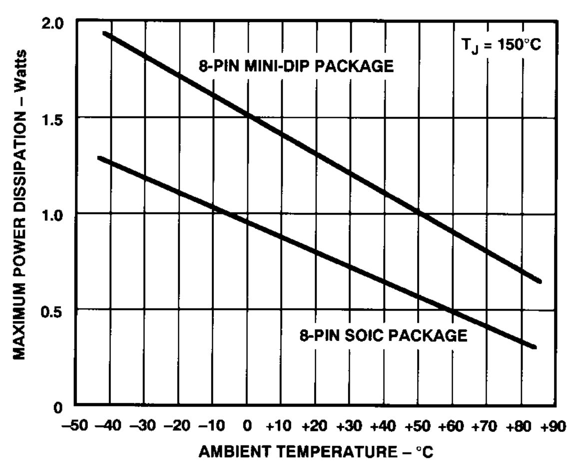
## ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic (N) . . . . . . . . . . . . . . . . . . . . See Derating Curves
  Small Outline (R) . . . . . . . . . . . . . . See Derating Curves
Input Voltage (Common Mode) . . . . . . . . . . . . . . . . . ±$V_S$
Differential Input Voltage . . . . . . . . . . . . . . . . . . . . ±6 V
Output Short Circuit Duration . . . . . . . . See Derating Curves
Storage Temperature Range (N, R) . . . . . . . −65°C to +125°C
Operating Temperature Range . . . . . . . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 10 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air: 8-pin plastic package, $\theta_{JA}$ = 90°C/watt; 8-pin SOIC package, $\theta_{JA}$ = 155°C/watt.

### ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD818AN | −40°C to +85°C | 8-Pin Plastic DIP | N-8 |
| AD818AR | −40°C to +85°C | 8-Pin Plastic SOIC | R-8 |
| AD818AR-REEL | −40°C to +85°C | 8-Pin Plastic SOIC | R-8 |



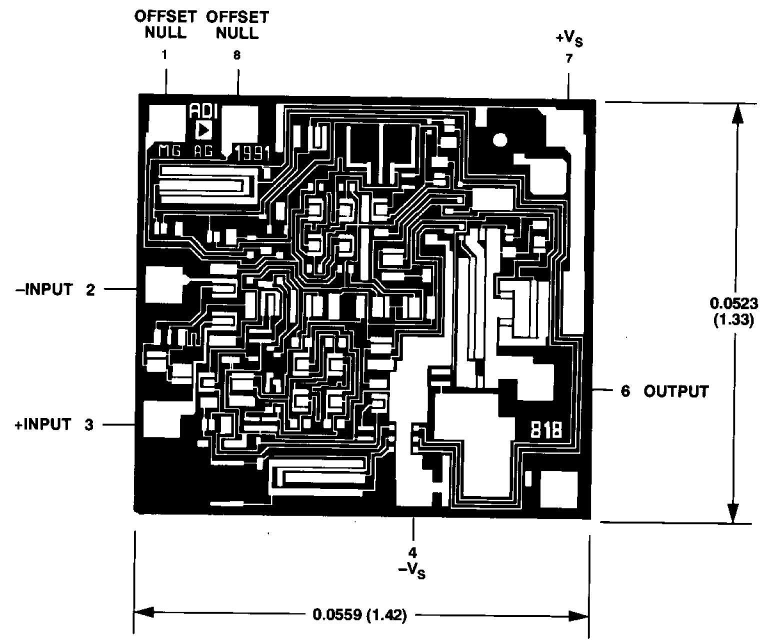

*Maximum Power Dissipation vs. Temperature for Different Package Types*

## ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD817 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

## METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



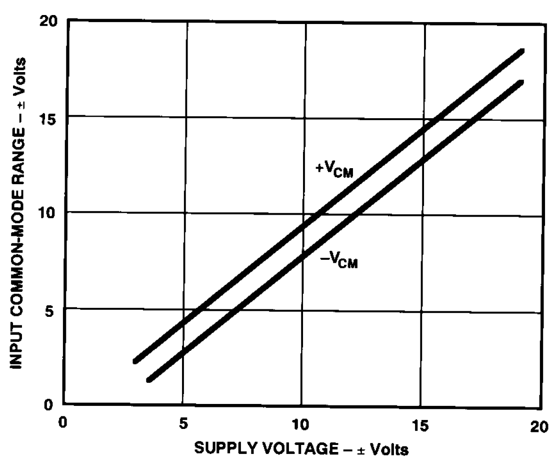




Figure 1. Common-Mode Voltage Range vs. Supply

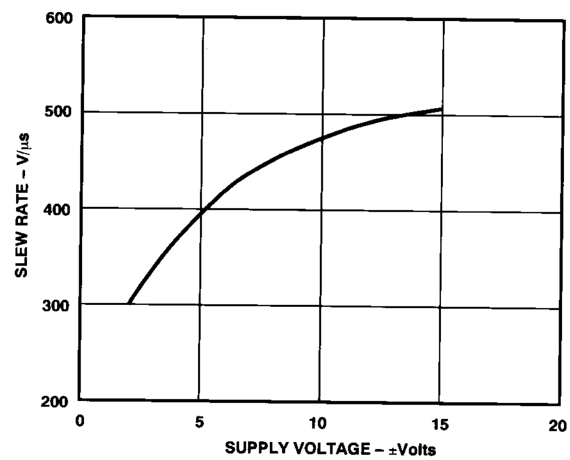



Figure 3. Slew Rate vs. Supply Voltage

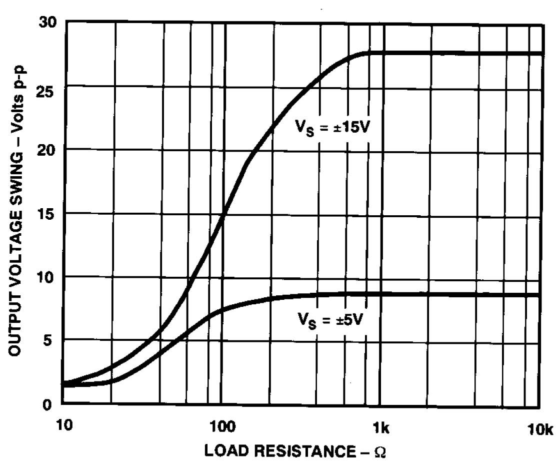



Figure 2. Output Voltage Swing vs. Load Resistance

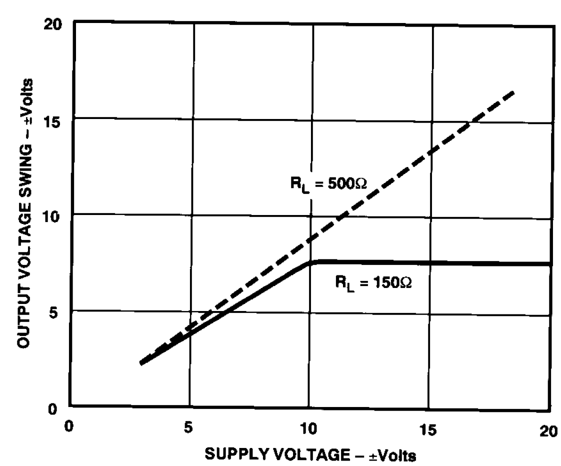



Figure 4. Output Voltage Swing vs. Supply

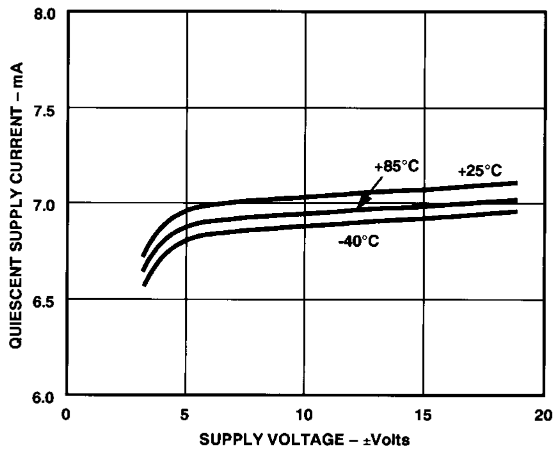



*Figure 5. Quiescent Supply Current vs. Supply Voltage*

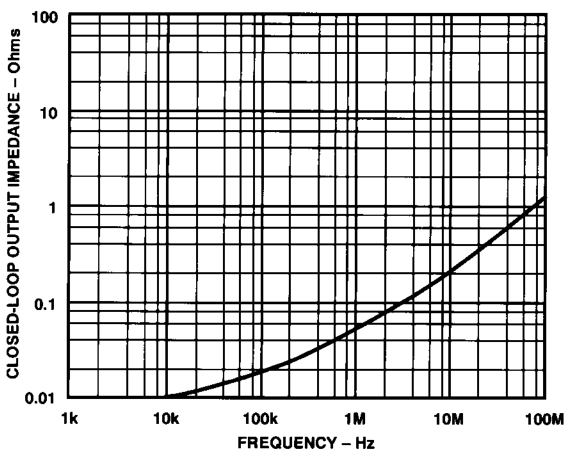



*Figure 6. Closed-Loop Output Impedance vs. Frequency*

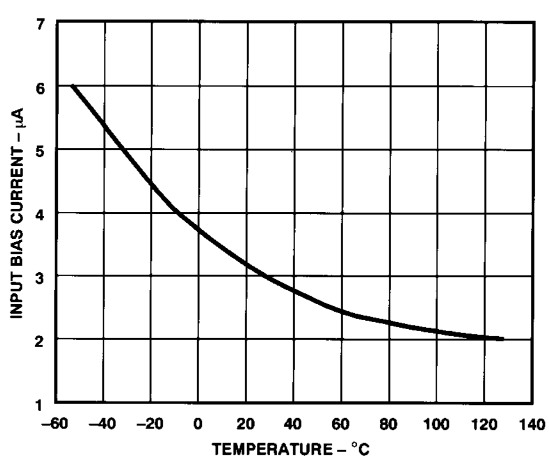



*Figure 7. Input Bias Current vs. Temperature*

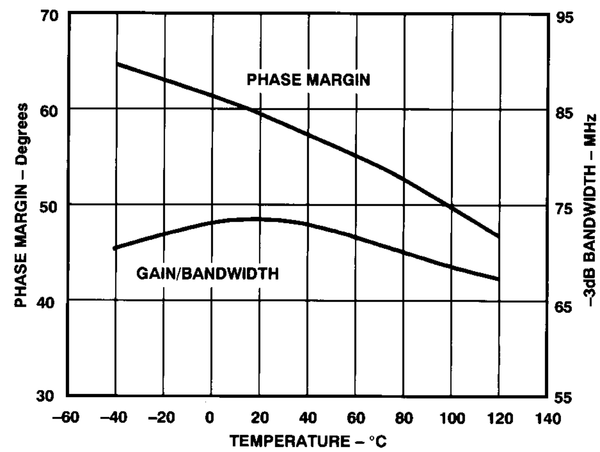



*Figure 8. −3 dB Bandwidth and Phase Margin vs. Temperature. Gain = +2*

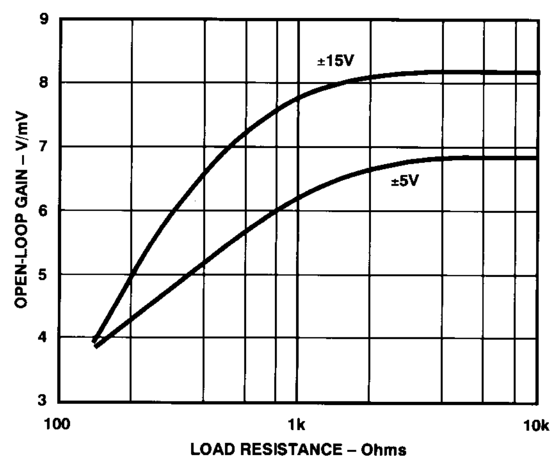



*Figure 9. Open-Loop Gain vs. Load Resistance*

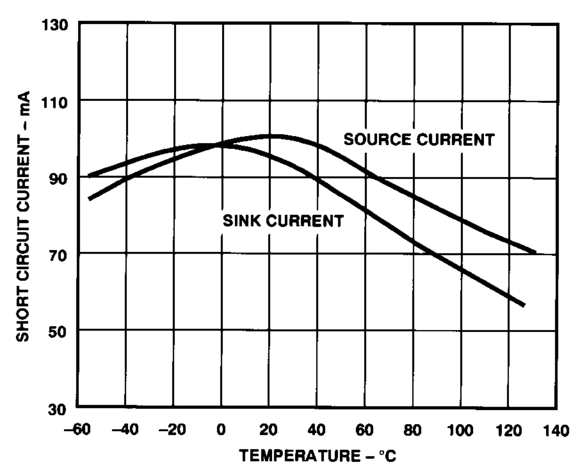



*Figure 10. Short Circuit Current vs. Temperature*

# AD818—Typical Characteristics

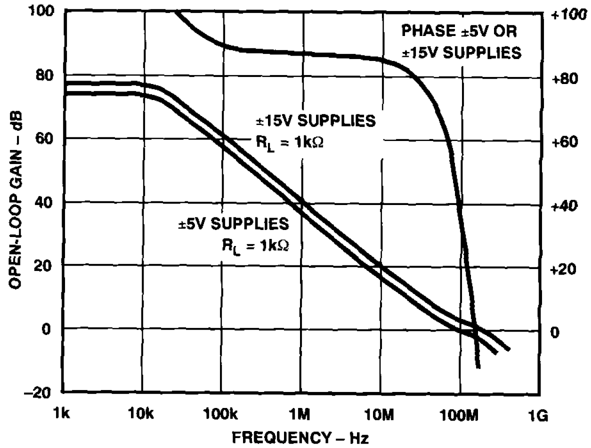



*Figure 11. Open-Loop Gain and Phase Margin vs. Frequency*

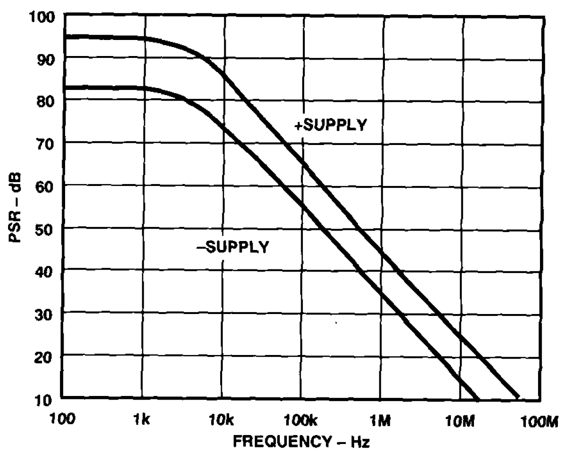



*Figure 12. Power Supply Rejection vs. Frequency*

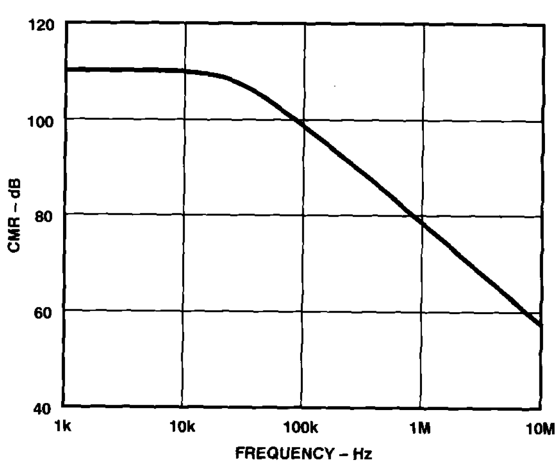



*Figure 13. Common-Mode Rejection vs. Frequency*

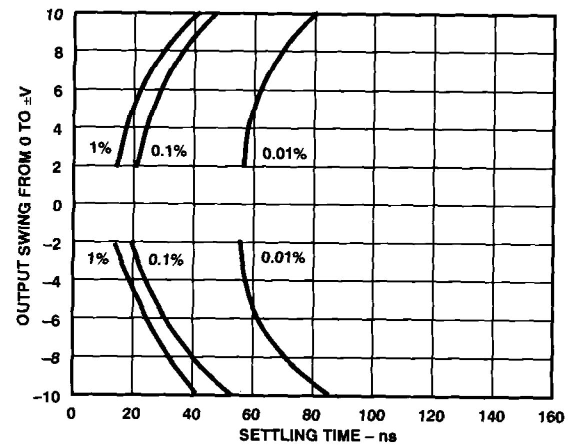



*Figure 14. Output Swing and Error vs. Settling Time*

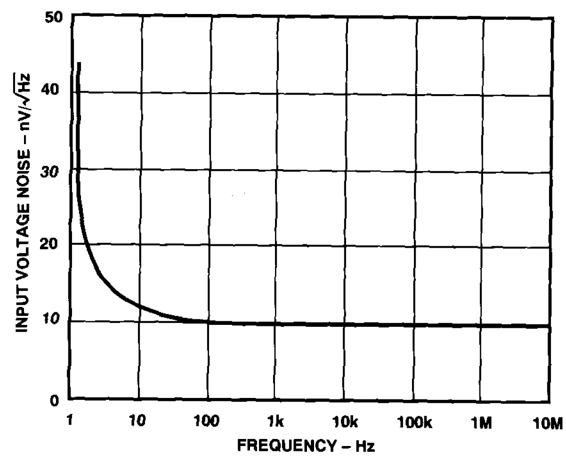



*Figure 15. Input Voltage Noise Spectral Density vs. Frequency*

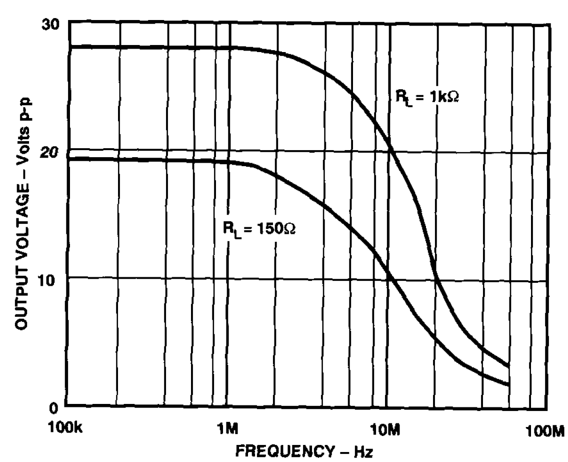



*Figure 16. Output Voltage vs. Frequency*

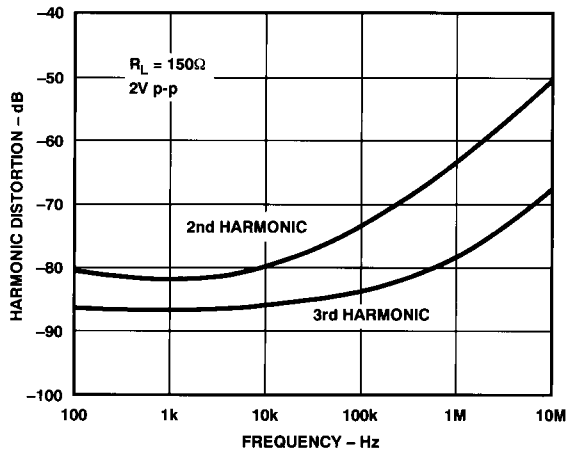



Figure 17. Harmonic Distortion vs. Frequency

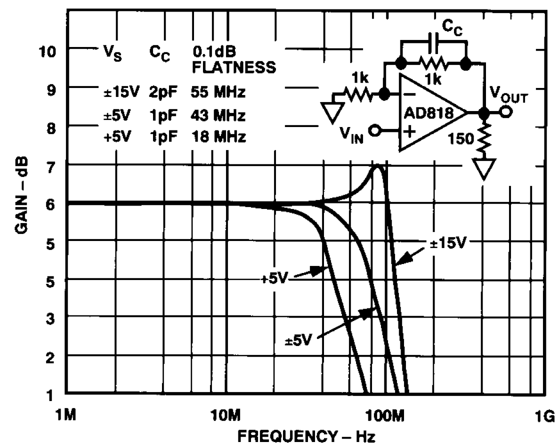



Figure 20. Closed-Loop Gain vs. Frequency (G = +2)

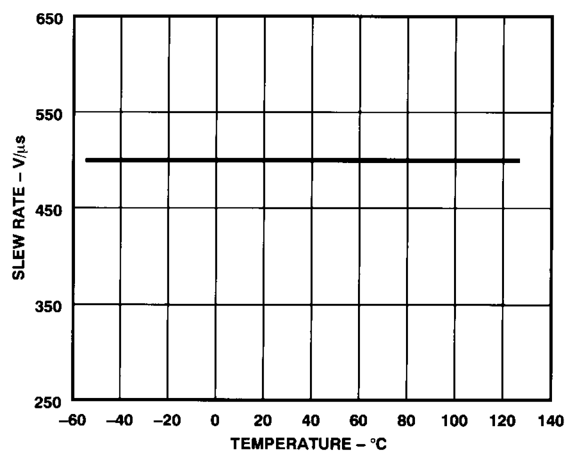



Figure 18. Slew Rate vs. Temperature

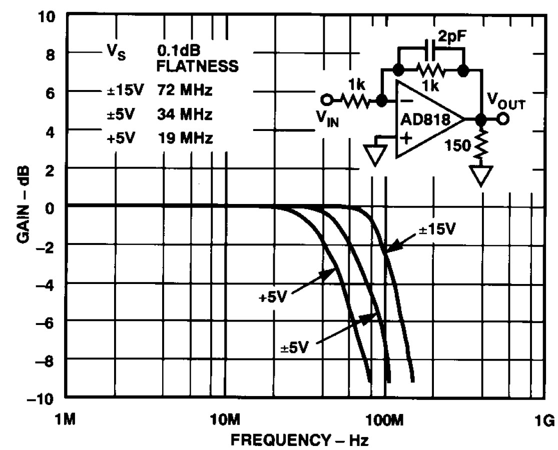



Figure 21. Closed-Loop Gain vs. Frequency (G = −1)

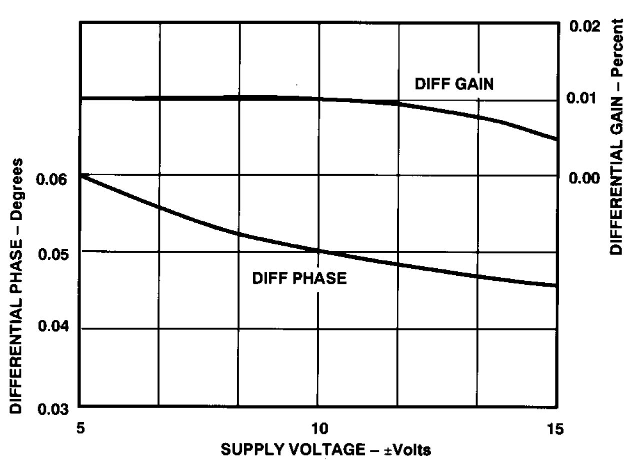



Figure 19. Differential Gain and Phase vs. Supply Voltage

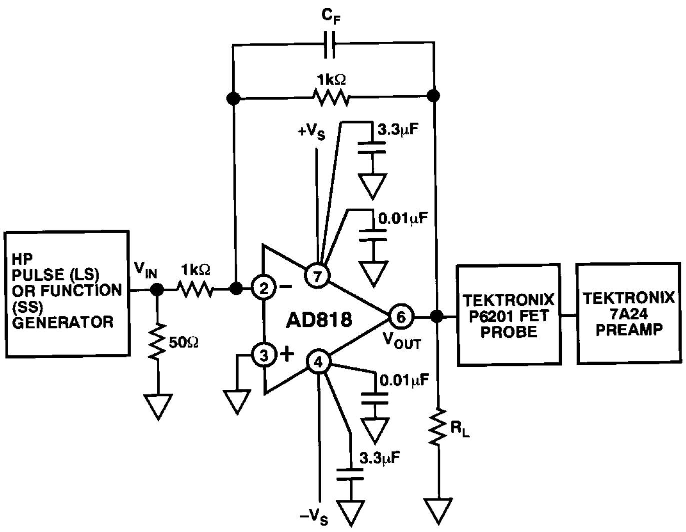



Figure 22. Inverting Amplifier Connection

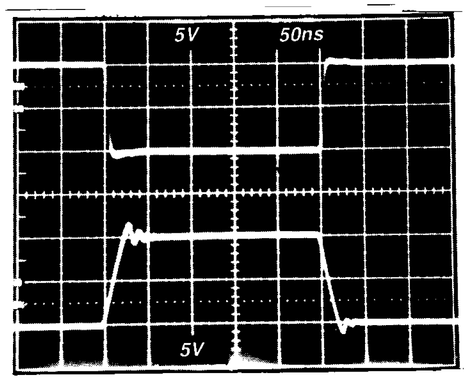



Figure 25. Inverter Large Signal Pulse Response $\pm 15\ V_S$, $C_F = 1\ pF$, $R_L = 1\ k\Omega$

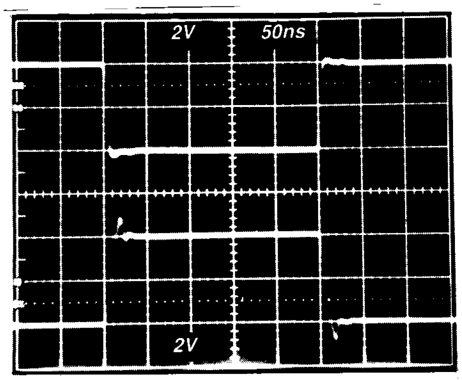



Figure 23. Inverter Large Signal Pulse Response $\pm 5\ V_S$, $C_F = 1\ pF$, $R_L = 1\ k\Omega$

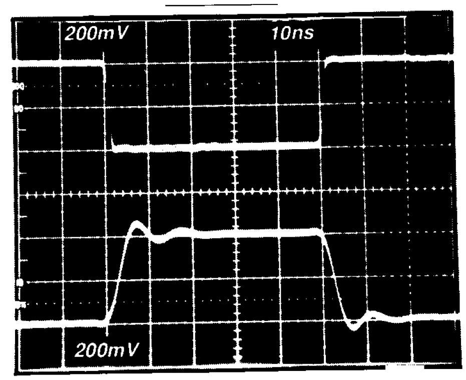



Figure 26. Inverter Small Signal Pulse Response $\pm 15\ V_S$, $C_F = 1\ pF$, $R_L = 150\ \Omega$

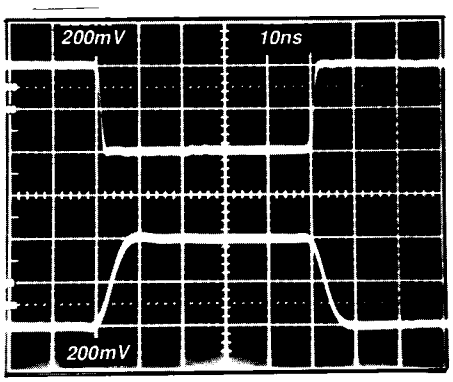



Figure 24. Inverter Small Signal Pulse Response $\pm 5\ V_S$, $C_F = 1\ pF$, $R_L = 150\ \Omega$

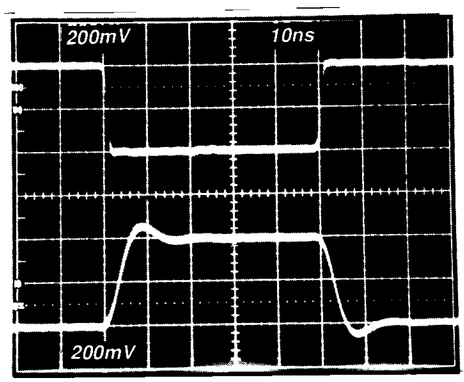



Figure 27. Inverter Small Signal Pulse Response $\pm 5\ V_S$, $C_F = 0\ pF$, $R_L = 150\ \Omega$

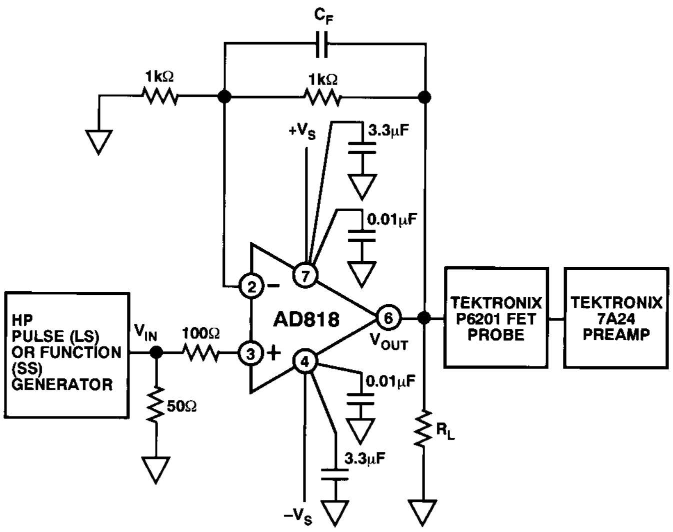



Figure 28. Noninverting Amplifier Connection

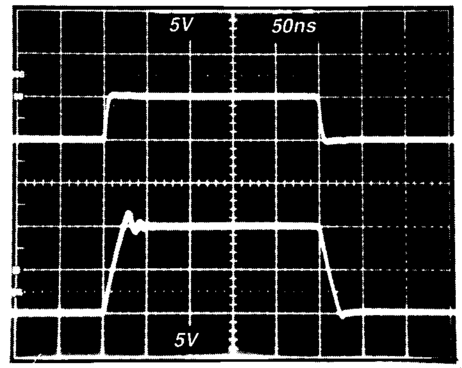



Figure 31. Noninverting Large Signal Pulse Response ±15 V, $C_F$ = 1 pF, $R_L$ = 1 kΩ

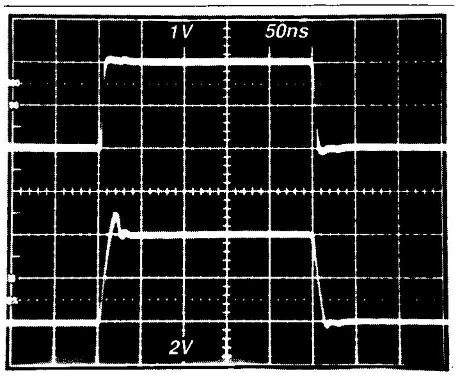



Figure 29. Noninverting Large Signal Pulse Response ±5 V, $C_F$ = 1 pF, $R_L$ = 1 kΩ

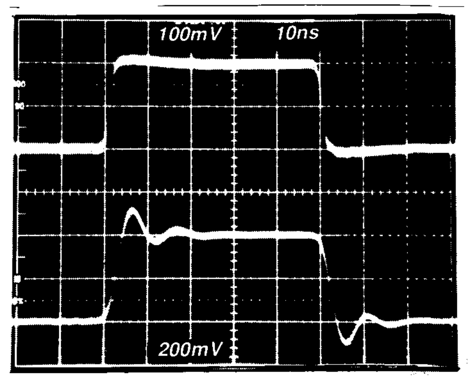



Figure 32. Noninverting Small Signal Pulse Response ±15 V, $C_F$ = 1 pF, $R_L$ = 150 Ω

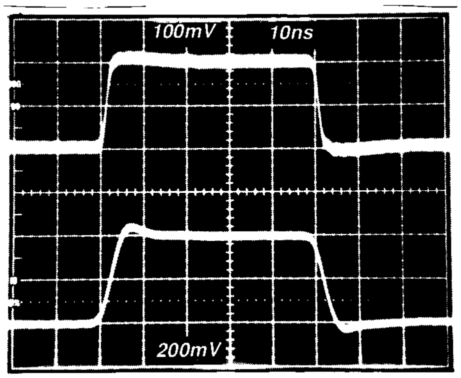



Figure 30. Noninverting Small Signal Pulse Response ±5 V, $C_F$ = 1 pF, $R_L$ = 150 Ω

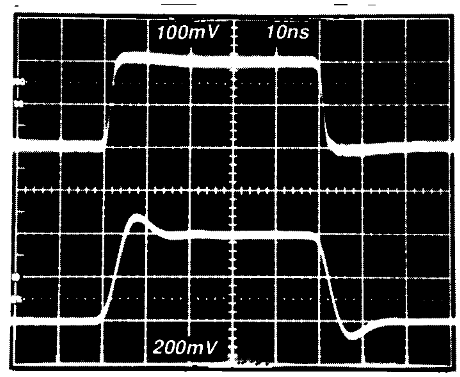



Figure 33. Noninverting Small Signal Pulse Response ±5 V, $C_F$ = 0 pF, $R_L$ = 150 Ω

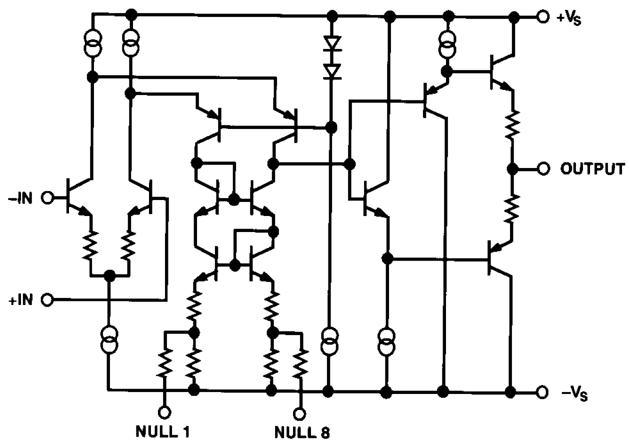



*Figure 34. AD818 Simplified Schematic*

## THEORY OF OPERATION

The AD818 is a low cost, video operational amplifier designed to excel in high performance, high output current video applications.

The AD818 (Figure 34) consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load, while maintaining low levels of distortion.

The AD818 will drive terminated cables and capacitive loads of 10 pF or less. As the closed-loop gain is increased, the AD818 will drive heavier cap loads without oscillating.

## INPUT CONSIDERATIONS

An input protection resistor ($R_{IN}$ in Figure 28) is required in circuits where the input to the AD818 will be subjected to transient of continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting their maximum base current.

For high performance circuits, it is recommended that a "balancing" resistor be used to reduce the offset errors caused by bias current flowing through the input and feedback resistors. The balancing resistor equals the parallel combination of $R_{IN}$ and $R_F$ and thus provides a matched impedance at each input terminal. The offset voltage error will then be reduced by more than an order of magnitude.

## GROUNDING AND BYPASSING

When designing high frequency circuits, some special precautions are in order. Circuits must be built with short interconnect leads. When wiring components, care should be taken to provide a low resistance, low inductance path to ground. Sockets should be avoided, since their increased interlead capacitance can degrade circuit bandwidth.

Feedback resistors should be of low enough value (≤1 kΩ) to assure that the time constant formed with the inherent stray capacitance at the amplifier's summing junction will not limit performance. This parasitic capacitance, along with the parallel resistance of $R_F/R_{IN}$, form a pole in the loop transmission which may result in peaking. A small capacitance (1–5 pF) may be used in parallel with the feedback resistor to neutralize this effect.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. Ceramic disc capacitors of 0.1 μF are recommended.

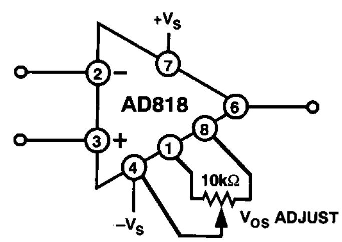



*Figure 35. Offset Null Configuration*

## OFFSET NULLING

The input offset voltage of the AD818 is inherently very low. However, if additional nulling is required, the circuit shown in Figure 35 can be used. The null range of the AD818 in this configuration is ±10 mV.

## SINGLE SUPPLY OPERATION

Another exciting feature of the AD818 is its ability to perform well in a single supply configuration. The AD818 is ideally suited for applications that require low power dissipation and high output current.

Referring to Figure 36, careful consideration should be given to the proper selection of component values. The choices for this particular circuit are: R1 + R3||R2 combine with C1 to form a low frequency corner of approximately 10 kHz. C4 was inserted in series with R4 to maintain amplifier stability at high frequency.

Combining R3 with C2 forms a low pass filter with a corner frequency of approximately 500 Hz. This is needed to maintain amplifier PSRR, since the supply is connected to $V_{IN}$ through the input divider. The values for R2 and C2 were chosen to demonstrate the AD818's exceptional output drive capability. In this configuration, the output is centered around 2.5 V. In order to eliminate the static dc current associated with this level, C3 was inserted in series with $R_L$.

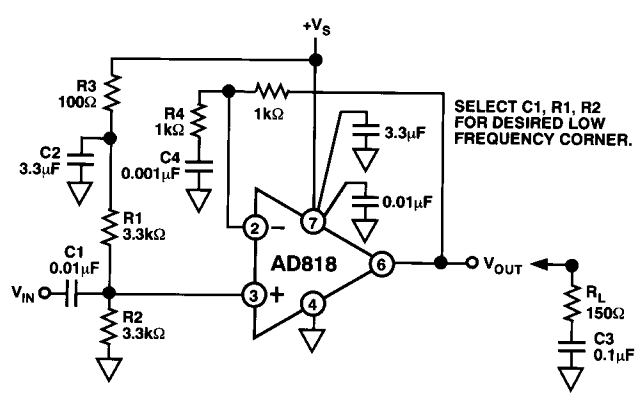



*Figure 36. Single Supply Amplifier Configuration*

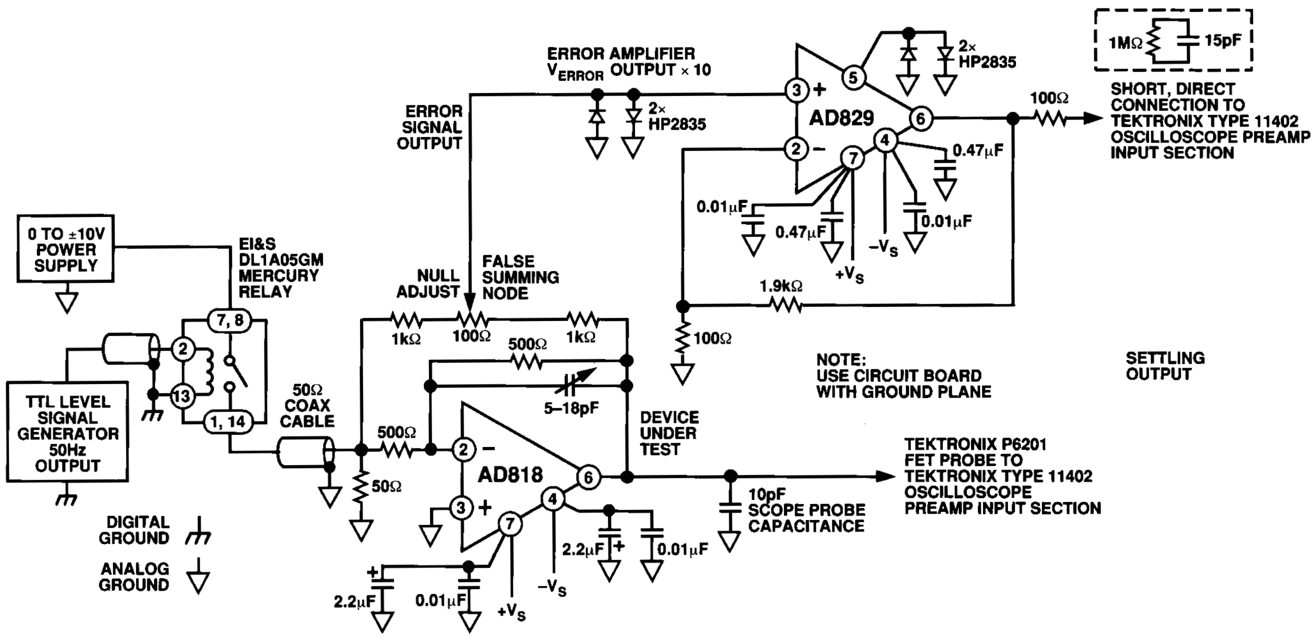



*Figure 37. Settling Time Test Circuit*

## AD818 SETTLING TIME

Settling time is comprised primarily of two regions. The first is the slew time in which the amplifier is overdriven, where the output voltage rate of change is at its maximum. The second is the linear time period required for the amplifier to settle to within a specified percent of the final value.

Measuring the rapid settling time of AD818 (45 ns to 0.1% and 80 ns to 0.01%—10 V step) requires applying an input pulse with a very fast edge and an extremely flat top. With the AD818 configured in a gain of −1, a clamped false summing junction responds when the output error is within the sum of two diode voltages (approximately 1 volt). The signal is then amplified 20 times by a clamped amplifier whose output is connected directly to a sampling oscilloscope.

### A High Performance Video Line Driver

The buffer circuit shown in Figure 38 will drive a back-terminated 75 Ω video line to standard video levels (1 V p-p) with 0.1 dB gain flatness to 55 MHz with only 0.05° and 0.01% differential phase and gain at the 3.58 MHz NTSC subcarrier frequency. This level of performance, which meets the requirements for high-definition video displays and test equipment, is achieved using only 7 mA quiescent current.

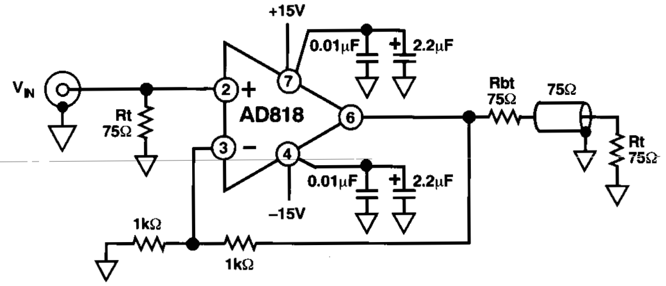



*Figure 38. Video Line Driver*

## DIFFERENTIAL LINE RECEIVER

The differential receiver circuit of Figure 39 is useful for many applications from audio to video. It allows extraction of a low level signal in the presence of common-mode noise. As shown in Figure 40, the AD818 provides this function with only $10nV/\sqrt{Hz}$ noise at the output.

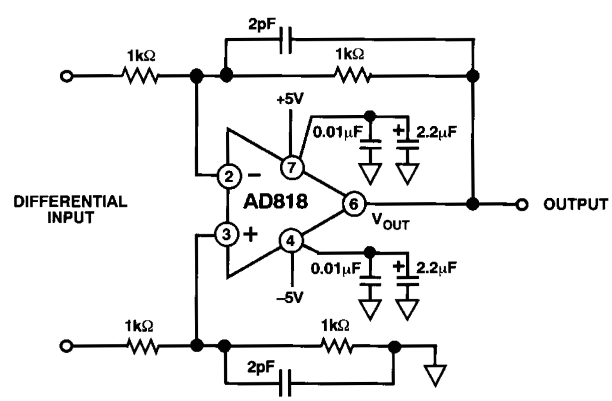



*Figure 39. Differential Line Receiver*

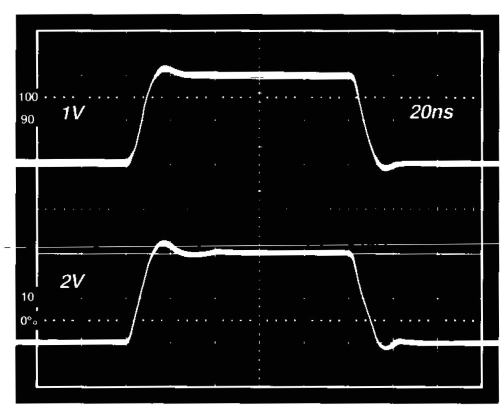
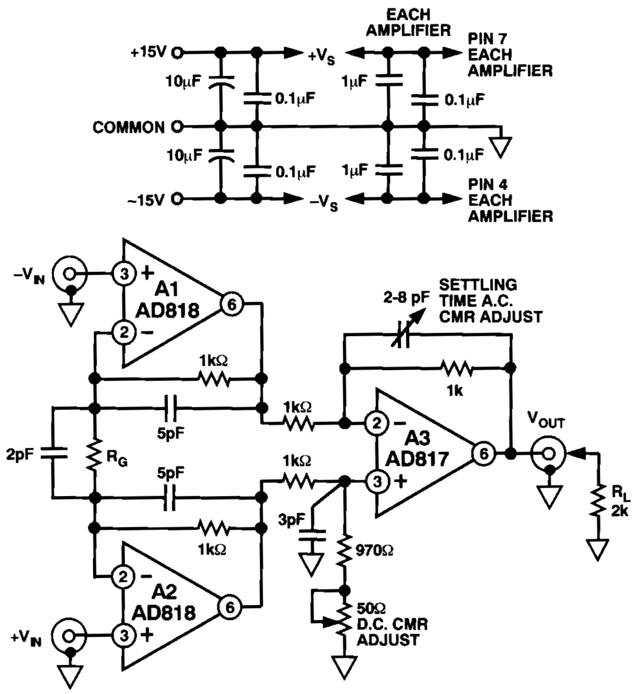



*Figure 40. Performance of Line Receiver, $R_L$ = 150 Ω, G = +2*

## A HIGH SPEED, THREE OP AMP IN AMP

The circuit of Figure 41 uses three high speed op amps: two AD818s and an AD817. This high speed circuit lends itself well to CCD imaging and other video speed applications. It has the optional flexibility of both dc and ac trims for common-mode rejection, plus the ability to adjust for minimum settling time.




BANDWIDTH, SETTLING TIME, & TOTAL HARMONIC DISTORTION VS. GAIN

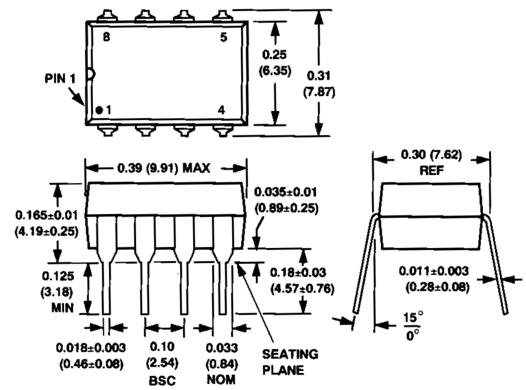
| GAIN | $R_G$ | CADJ (pF) | SMALL SIGNAL BANDWIDTH | SETTLING TIME TO 0.1% | THD + NOISE BELOW INPUT LEVEL @ 10kHz |
|---|---|---|---|---|---|
| 3 | 1k | 2-8 | 14.7 MHz | 200ns | 82 dB |
| 10 | 222Ω | 2-8 | 4.5 MHz | 370ns | 81 dB |
| 100 | 20Ω | 2-8 | 960 kHz | 2.5μs | 71 dB |

*Figure 41. High Speed 3 Op Amp In Amp*

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 8-Pin Plastic Mini-DIP (N) Package




### 8-Pin SOIC (R) Package

